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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/609,892	06/30/2003	Marcus A. Baker	RPS920030073US1	8340

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EXAMINER	
URICK, MATTHEW T	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 03/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/609,892	BAKER ET AL.	
	Examiner	Art Unit	
	Matt Urick	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

NON-FINAL OFFICIAL ACTION

Status of the Claims

Claims 1, 2, 6, 8, 10, 13-15, 17-20, 23, 25-28, and 30-33, and 35 are rejected under 35 USC 102

Claims 3, 4, 5, 7, 9, 11, 12, 16, 21, 22, 24, 29, 34, and 36 are rejected under 35 USC 103

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 6, 8, 10, 13-15, 17-20, 23, 25-28, and 30-33, and 35 are rejected under 35 U.S.C. 102(b) as being anticipated by Vachon (United States Patent Application Publication No. 2002/0078404 A1).

As per claim 1, Vachon discloses:

A system for saving the state of an integrated circuit, the system comprising:

a non-volatile memory (¶ 25 lines 4-9, and ¶ 31 lines 8-10: the computing system for typical use in this invention contains a hard disk); and

a state-saving controller coupled to the non-volatile memory and coupled to the integrated circuit, wherein the state-saving controller saves the state of the integrated circuit to the non-volatile memory when a failure occurs in the integrated circuit (¶ 34 a

crash dump file is created when a failure is detected).

As per claim 2, Vachon discloses:

The system of claim 1 wherein the state-saving controller saves the state of substantially all latches of the integrated circuit to the non-volatile memory when a failure occurs in the integrated circuit (¶ 33 last 6 lines).

As per claim 6, Vachon discloses:

The system of claim 1 wherein the state-saving controller is a separate component electrically coupled to the integrated circuit and to the non-volatile memory via a bus (¶ 32 - ¶ 33 host computer is a separate component which is connected to target computer via a serial bus).

As per claim 8, Vachon discloses:

The system of claim 6 wherein the bus is a serial bus (¶ 32 - ¶ 33 host computer is a separate component which is connected to target computer via a serial bus).

As per claim 10, Vachon discloses:

The system of claim 1 wherein the non-volatile memory is a separate component electrically coupled to the integrated circuit by a bus (¶ 32 - ¶ 33 host computer is a separate component which is connected to target computer via a serial bus).

As per claim 13, Vachon discloses:

The system of claim 1 wherein the saved state of the integrated circuit includes the data contents of registers and other latches of the integrated circuit (¶ 33 last 6 lines: all of target computer's memory is saved).

Claim 14 is rejected as the method of using the system of claim 1.

Claim 15 is rejected as the method of using the system of claim 2.

As per claim 17, Vachon discloses:

The method of claim 14 wherein all internal clocks of the integrated circuit are stopped so that the latches retain their states upon the error in the operation of the integrated circuit (¶ 38: Vachon discloses that all operations are halted for the duration of the memory dump, and ¶ 9 operations are commonly halted in memory dump scenarios).

As per claim 18, Vachon discloses:

The method of claim 14 wherein an error flag is asserted after the state of the integrated circuit has been saved (¶ 38 last 7 lines: target computer resumes operation and host computer begins debugging after memory dump is completed).

As per claim 19, Vachon discloses:

The method of claim 18 wherein the error flag is provided to a service processor monitoring the operation of the integrated circuit saved (¶ 38 last 7 lines: host computer begins debugging after memory dump is completed).

Claim 20 is rejected as the method of using the system of claim 6.

Claim 23 is rejected as the method of using the system of claim 10.

As per claim 25, Vachon discloses:

The method of claim 14 wherein the state of the integrated circuit is saved automatically upon the occurrence of the error, without receiving a request to save the state from a source outside the integrated circuit and state-saving controller (¶ 38 the crash dump file is created through a DMA command).

Claim 26 is rejected as the method of using the system of claim 13.

Claim 27 is rejected as a computer readable medium of using the system of claim 1.

Claim 28 is rejected as a computer readable medium of using the system of claim 2.

Claim 30 is rejected as a computer readable medium of using the method of claim 17.

Claim 31 is rejected as a computer readable medium of using the method of claim 18.

Claim 32 is rejected as a computer readable medium of using the method of claim 19.

Claim 33 is rejected as a computer readable medium of using the system of claim 6.

Claim 35 is rejected as a computer readable medium of using the system of claim 10.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 9, 11, 16, 24, 29, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vachon (United States Patent Application Publication No. **2002/0078404 A1**) in view of Vachon (United States Patent No. **6,681,348 B1**).

As per claim 3, Vachon 404 discloses:

The system of claim 1 wherein the state of each latch is saved (¶ 33 last 6 lines).

Vachon 404 fails to disclose:

. . . when the failure is an unrecoverable error in the integrated circuit.

Although Vachon 404 fails to specifically disclose that crash dump files are generated for fatal errors, Vachon 348 discloses that crash dump files are generated when the system physically "crashes" (column 1 lines 14-30). Since Vachon 348 is saving crash dump files for the purposes of debugging (column 2 lines 18-27), and Vachon 404 also uses crash dump files for debugging (¶ 1), it would be obvious to use them for various types of errors, including crashes. Therefore, it would have been obvious to one of ordinary skill in the art to use Vachon 404's crash dump files for system crashes as disclosed by Vachon 348.

As per claim 9, Vachon 404 fails to disclose:

The system of claim 1 wherein the state-saving controller is integrated with and internal to the integrated circuit.

Vachon 348 discloses a system in which a machine runs a crash dump process and stores a crash dump file to a location within the machine's physical memory (column 4 lines 47-51: describing machine 10). Vachon 348 discloses that sometimes it may be inefficient or not possible to transmit the crash dump file over an external link (column 1 lines 57-59). Vachon 404 also discloses that remotely storing a crash dump file may create time constraints (¶ 5). Storing it within the computer would prevent this bottleneck from occurring. Therefore, it would have been obvious to one of ordinary skill in the art to use Vachon 404's local crash dump file storage for system crashes as disclosed by Vachon 348.

As per claim 11, Vachon 404 fails to disclose:

The system of claim 1 wherein the non-volatile memory is integrated with and internal to the integrated circuit.

Vachon 348 discloses a system in which a machine runs a crash dump process and stores a crash dump file to a location within the machine's physical memory (column 4 lines 47-51: describing machine 10). Vachon 348 discloses that sometimes it may be inefficient or not possible to transmit the crash dump file over an external link (column 1 lines 57-59). Vachon 404 also discloses that remotely storing a crash dump

file may create time constraints (¶ 5). Storing it within the computer would prevent this bottleneck from occurring. Therefore, it would have been obvious to one of ordinary skill in the art to use Vachon 404's local crash dump file storage for system crashes as disclosed by Vachon 348.

Claim 16 is rejected as the method of using the system of claim 3.

Claim 24 is rejected as the method for using the system of claim 11.

Claim 29 is rejected as a computer readable medium of using the system of claim 3.

Claim 36 is rejected as the computer readable medium of the system of claim 9.

Claims 4 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vachon (United States Patent Application Publication No. 2002/0078404 A1) in view of Powley (European Silicon Structures Limited: The Beginner's Guide To ASICs).

As per claim 4, Vachon fails to disclose:

The system of claim 1 wherein the integrated circuit is an Application Specific Integrated Circuit (ASIC).

Powley discloses the benefits of implementing a system on an ASIC chip, such as reduced cost, higher reliability, reduced testing, reduced power consumption (page 2: "What are the Benefits of ASICs?"). Powley also discloses that a printed circuit board can be easily copied and implemented as a ASIC. Vachon discusses the time-

constraints of debugging (Vachon ¶ 10). Implementing the target computer of Vachon's invention as an ASIC would improve the reliability, speed and cost of the process, making it more efficient and less time-intensive. Therefore, it would have been obvious to one of ordinary skill in the art to incorporate ASICs into the crash dump system of Vachon, creating a more reliable and efficient process.

Claim 21 is rejected as the method of using the system of claim 4.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vachon (United States Patent Application Publication No. 2002/0078404 A1) in view of Microsoft Computer Dictionary (fifth edition).

Vachon fails to disclose:

The system of claim 1 wherein the non-volatile memory is an Electrically-Erasable Programmable Read Only Memory (EEPROM).

Microsoft Computer Dicitonary defines an EEPROM as a non-volatile storage medium which can be erased with an electrical signal when desired. It can be useful for long term storage. Vachon discloses that any type of nonvolatile storage may be used in his system (¶ 25 lines 10-25). Using an EEPROM would be a suitable memory that is both reprogrammable and nonvolatile. Therefore, it would have been obvious to one of ordinary skill in the art to incorporate EEPROM into the crash dump system of Vachon, as a means for nonvolatile storage.

Claims 7, 12, 22, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vachon (United States Patent Application Publication No. 2002/0078404 A1) in view of Masuyama (United States Patent Application Publication No. 2003/0145142 A1).

As per claim 7, Vachon fails to disclose:

The system of claim 6 wherein the state-saving controller is a bus master of the bus.

Masuyama discloses a system in which multiple subsystems are connected to a management controller by a bus (¶ 5 - ¶ 11). Each subsystem stores crash dump files when there is an error in the system, and must wait for a request signal from the management controller before they can be sent over the bus (¶ 10). In this way, the management controller acts as a state saving controller and a bus master. Masuyama discloses that this enables one management controller to monitor several subsystems at once, without the cost of multiple interfaces or excessive data transfer (¶ 2 lines 9-17). Vachon also discloses that he wishes to limit data transfer (Vachon column 1 lines 31-40). Using Masuyama's management controller would help reduce the cost of monitoring multiple subsystems and storing their respective crash dump files, and reduce the time involved in sending and storing them. Therefore, it would have been obvious to one of ordinary skill in the art to incorporate the management controller of Masuyama into the crash dump system of Vachon, increasing the cost efficiency and reducing the transmission time of crash dump files.

As per claim 12, Vachon fails to disclose:

The system of claim 1 further comprising at least one additional integrated circuit, wherein the additional integrated circuit is coupled to the non-volatile memory and to the state-saving controller, and wherein the state-saving controller saves the state of the additional integrated circuit to the non-volatile memory when a failure occurs in the additional integrated circuit.

Masuyama discloses a system in which multiple subsystems are connected to a management controller by a bus (¶ 5 - ¶ 11). Each subsystem stores crash dump files when there is an error in the system, and must wait for a request signal from the management controller before they can be sent over the bus (¶ 10). Masuyama discloses that this enables one management controller to monitor several subsystems at once, without the cost of multiple interfaces or excessive data transfer (¶ 2 lines 9-17). Vachon also discloses that he wishes to limit data transfer (Vachon column 1 lines 31-40). Using Masuyama's management controller would help reduce the cost of monitoring multiple subsystems and storing their respective crash dump files, and reduce the time involved in sending and storing them. Therefore, it would have been obvious to one of ordinary skill in the art to incorporate the management controller of Masuyama into the crash dump system of Vachon, increasing the cost efficiency and reducing the transmission time of crash dump files.

Claim 22 is rejected as the method for using the system of claim 12.

Claim 34 is rejected as the method for using the system of claim 12.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matt Urick whose telephone number is (571) 272-0805. The examiner can normally be reached on 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Bryce P. Bonzo

BRYCE P. BONZO
PRIMARY EXAMINER

MTU

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